R20

Course Code: 20EC4202

SIDDHARTH INSTITUTE OF ENGINEEERING & TECHNOLOGY:: PUTTUR

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QUESTION BANK (DESCRIPTIVE)

Subject with Code : DICD (20EC4202) **Course & Branch**: M.Tech-VLSI

Year &Sem: I-M.Tech & I-Sem **Regulation:** R20

UNIT-I
CMOS INVERTER & LOGIC

1	a)	Draw the circuit for NMOS inverter and explain its operation.	[L1] [CO1]	6M
	b)	Compare the characteristics of the different types of MOS inverters in terms of noise margin and power dissipation.	[L2] [CO1]	6M
2	a)	What makes dynamic CMOS circuits faster than static CMOS circuits?	[L1] [CO1]	6M
	b)	Draw the ideal characteristics of a CMOS inverter and compare it with the actual characteristics.	[L1] [CO1]	6M
3		Design a static CMOS circuit to realize the following functions:		
	a)	F = b + (a • c) + ca.	[L6] [CO2]	6M
	b)	XNOR gate.	[L6] [CO2]	6M
4	a)	Draw the circuit topology and explain the operation of CMOS domino logic.	[L1] [CO1]	6M
	b)	How clock skew problem is overcomes in domino CMOS circuits?	[L1] [CO1]	6M
5	a)	Implement the 2-input NAND gate with CMOS logic and explain its working.	[L6] [CO2]	6M
	b)	What are the advantages of dynamic logic over static CMOS logic?	[L1] [CO1]	6M
6	a)	With the help of diagrams, explain about static CMOS inverter.	[L2] [CO1]	6M
	b)	Discuss about the performance of dynamic CMOS inverter.	[L6] [CO1]	6M
7	a)	Implement the 2-input NOR gate with static CMOS and dynamic CMOS.	[L6] [CO2]	6M
	b)	How clock skew problem is overcome in NORA CMOS circuits?	[L1] [CO1]	6M
8	a)	Construct a XNOR gate in dynamic logic and explain its working.	[L3] [CO2]	6M
	b)	What are the problems associated with dynamic logic?	[L1] [CO1]	6M
9	a)	How does the domino logic solves the problem in dynamic logic?	[L1] [CO1]	6M
	b)	In which way NORA logic is power efficient? Explain with appropriate equations.	[L2] [CO1]	6M
10	a)	Design 4-to-1 MUX using CMOS transmission gate.	[L6] [CO2]	6M
	b)	Compare the sources of power dissipation between static CMOS and dynamic CMOS.	[L2] [CO1]	6M

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UNIT-II
CMOS DESIGN

1	a)	Illustrate the method of logical effort for transistor sizing.	[L2] [CO4]	6M
	b)	Explain the read/write operation of the SRAM cell.	[L2] [CO2]	6M
2		Prove that the delay of a series of pass transistors can be reduced from quadratic dependence to linear dependence on the number of transistors in series by inserting buffers at suitable intervals.	[L5] [CO3]	12M
3	a)	Explain about different strategies for building low power CMOS gates.	[L2] [CO2]	6M
	b)	Draw the circuit for 4 transistors SRAM and explain its working.	[L1] [CO2]	6M
4	a)	Why low power has become an important issue in the present day VLSI circuit realization?	[L1] [CO2]	6M
	b)	Explain how read and write operations are performed in a SRAM.	[L2] [CO2]	6M
5	a)	Sketch the schematic diagram of a SRAM memory cell along with sense amplifier and data write circuitry.	[L1] [CO2]	6M
	b)	Discuss about power consumption in CMOS gates.	[L6] [CO2]	6M
6	a)	What is meant by logical effort?	[L1] [CO4]	6M
	b)	Explain the design considerations of a 4-bit SRAM with the help of CMOS logic diagram.	[L2] [CO2]	6M
7	a)	Explain the logical effort of two – input NAND and NOR gates with neat circuit diagram.	[L2] [CO4]	6M
	b)	In what way the DRAMs differ from SRAMs?	[L1] [CO2]	6M
8	a)	Explain about different strategies for building low power CMOS gates.	[L2] [CO2]	6M
	b)	Explain the read and write operations for a one transistor DRAM cell.	[L2] [CO2]	6M
9	a)	Explain with a neat sketch about the operation of the 6 transistor SRAM cell.	[L2] [CO2]	6M
	b)	Explain the design considerations of a 4-bit RAM with the help of CMOS logic diagram.	[L2] [CO2]	6M
10	a)	What is short circuit power dissipation? On what parameters does it depend?	[L1] [CO2]	6M
	b)	Draw one cell dynamic RAM circuit and explain its working.	[L1] [CO2]	6M

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UNIT-III
BIPOLAR GATE DESIGN

1		What is dynamic behavior of BiCMOS logic? Explain in detail with neat sketches.	[L1] [CO3]	12M
2		Draw the schematic diagram of different Bi-CMOS inverters. Explain its operation.	[L1] [CO3]	12M
3	a)	Compare the switching characteristics of a BiCMOS inverter with respect to that for static CMOS for different fan out conditions.	[L2] [CO3]	6M
	b)	Design NAND gate in BiCMOS logic.	[L6] [CO3]	6M
4	a)	Explain how to calculate the delay for the BiCMOS circuits.	[L2] [CO3]	6M
	b)	Explain the concept of BiCMOS inverter.	[L2] [CO3]	6M
5		Explain in detail how do we calculate power for BiCMOS and on what parameters the power equation depends on?	[L2] [CO3]	12M
6		Draw and explain the static and dynamic characteristics of BICMOS inverter.	[L1] [CO3]	12M
7	a)	Discuss about delay and power consumption in BICMOS logic circuits.	[L6] [CO3]	6M
	b)	List the advantages and disadvantages of Bi-CMOS.	[L4] [CO3]	6M
8		Explain the working principle of Bi-CMOS with the help of static and dynamic characteristics.	[L2] [CO3]	12M
9		Explain about bipolar gate design in detail with neat sketches.	[L2] [CO3]	12M
10		What is static behavior of Bi-CMOS logic? Explain in detail with neat sketches.	[L1] [CO3]	12M

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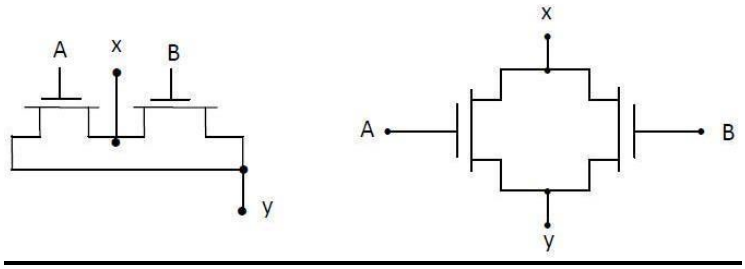
UNIT-IV
LAYOUT DESIGN RULES

1	a)	What are the general observations on the design rules?	[L1] [CO4]	6M
	b)	Write about NMOS based design rules.	[L1] [CO4]	6M
2	a)	Discuss about 'Mead Conway Design' rules for silicon gate NMOS process.	[L6] [CO4]	8M
	b)	What is the need for design rules? Explain.	[L1] [CO4]	4M
3		Design a CMOS logic gates for the function $F = \overline{(A+BC)}.\ \overline{D}$. Also indicate the connections of signals F, V_{DD} and GND. Draw the stick diagram representation for the circuit designed.	[L6] [CO4]	12M
4	a)	What are the CMOS based design rules?	[L1] [CO4]	6M
	b)	Explain two input NAND gate with relevant Layout example.	[L2] [CO4]	6M
5		Draw the stick diagram for the following schematic using appropriate colors. 	[L1] [CO4]	12M
6		Write about:		
	a)	Area capacitance	[L1] [CO4]	6M
	b)	Drive large capacitive load	[L1] [CO4]	6M
7	a)	What is the need of wired capacitance? Where it is used? Explain.	[L1] [CO4]	6M
	b)	What is area capacitance? Explain its significance in the layout design.	[L1] [CO4]	6M
8		Write about:		
	a)	Sheet resistance	[L1] [CO4]	6M
	b)	Lambda based design rules	[L1] [CO4]	6M
9	a)	What is sheet resistance? Find out the expression fo the resistance of rectangular sheet in terms of sheet resistance.	[L1] [CO4]	6M
	b)	Find out the capacitance of a MOS capacitor.	[L1] [CO4]	6M
10	a)	Implement the 2-input XOR gate for CMOS logic and explain its working.	[L6] [CO2]	6M
	b)	Design Layout Diagram for above diagram with relevant colors.	[L6] [CO4]	6M

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UNIT-V
SUBSYSTEM DESIGN PROCESS

1	a)	How to design a 4-bit shifter? Explain with schematic.	[L1] [CO5]	6M
	b)	What is pipeline multiplier array? Explain.	[L1] [CO5]	6M
2	a)	Discuss about design approach of carry look ahead adder with neat sketch.	[L6] [CO5]	6M
	b)	Explain Booth's algorithm and its modified algorithm.	[L2] [CO5]	6M
3	a)	Compare different types of CMOS subsystem shifters.	[L5] [CO5]	6M
	b)	Discuss about design approach of 4-bit shifter.	[L6] [CO5]	6M
4	a)	Draw and explain the booth decode cell used for booth multiplier.	[L1] [CO5]	6M
	b)	Design a 4-bit CLA adder.	[L6] [CO5]	6M
5	a)	Analyze the timing of this 4-bit CLA.	[L4] [CO5]	6M
	b)	Compare CLA with RCA and state its merits and demerits.	[L6] [CO5]	6M
6	a)	Draw the circuit diagram of 4-bit Baugh-Wooley multiplier structure and explain.	[L1] [CO6]	6M
	b)	Comment on the advantages and disadvantages of the multiplier.	[L4] [CO6]	6M
7	a)	How to design the ALU sub-system? Give the process.	[L1] [CO6]	6M
	b)	Design the sub-system Serial Parallel Multiplier.	[L6] [CO6]	6M
8	a)	Analyze the timing of the array multiplier.	[L4] [CO6]	6M
	b)	Explain the modified booth algorithm.	[L2] [CO5]	6M
9	a)	Construct 4-bit SISO and explain its operations.	[L6] [CO5]	6M
	b)	With a neat sketch explain the working of array multiplier.	[L2] [CO5]	6M
10	a)	Design the circuit diagram of logarithmic shifter using CMOS logic.	[L6] [CO5]	6M
	b)	Explain what is subsystem design process.	[L2] [CO5]	6M

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